A Comparison of Silicon UMOSFETs Versus GaAs Vertical FETs For Low Voltage, Synchronous Rectification at 2.5 MHz[1]

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Abstract

A comparison between the rectification efficiency of silicon UMOSFETs versus GaAs vertical FETs in a 1.5 volt, 2.5 megahertz power supply application is presented. A new figure of merit describing conduction and switching losses of synchronous rectifiers in a resonant circuit is developed to compare losses. A method to minimize losses by optimizing die area is discussed. A summary of present silicon and GaAs vertical channel FET technology is presented. Theoretical and experimental results are reported for the best silicon UMOSFET and GaAs VFET designs. It is shown that the GaAs VFET is substantially more efficient with approximately 1/3 the loss of the silicon approach.

1.0 INTRODUCTION

With the rapid increases in gate packing density, higher operating speeds and advanced packaging techniques such as multi-chip modules, there is continuing pressure for power supply densities to increase. Figure 1 shows the trend for a power supply to occupy a reasonable portion of the volume of an electronic system. State of the art packaging technology and logic circuits require power supply densities in the 10 watts per cubic inch range. With the advent of submicron logic devices and multichip module packaging techniques, power supply density requirements may reach 100 watts per cubic inch by the turn of the century.

As power supply power densities are increased, power dissipating components are moved closer together making cooling a larger problem. Higher efficiencies will be required to maintain junction temperatures for reliable designs. In low voltage power supplies, the output rectifier is usually the highest loss element. Schottky or junction diodes have a fixed forward junction voltage which limits their efficiency, particularly in low voltage power supplies. Synchronous

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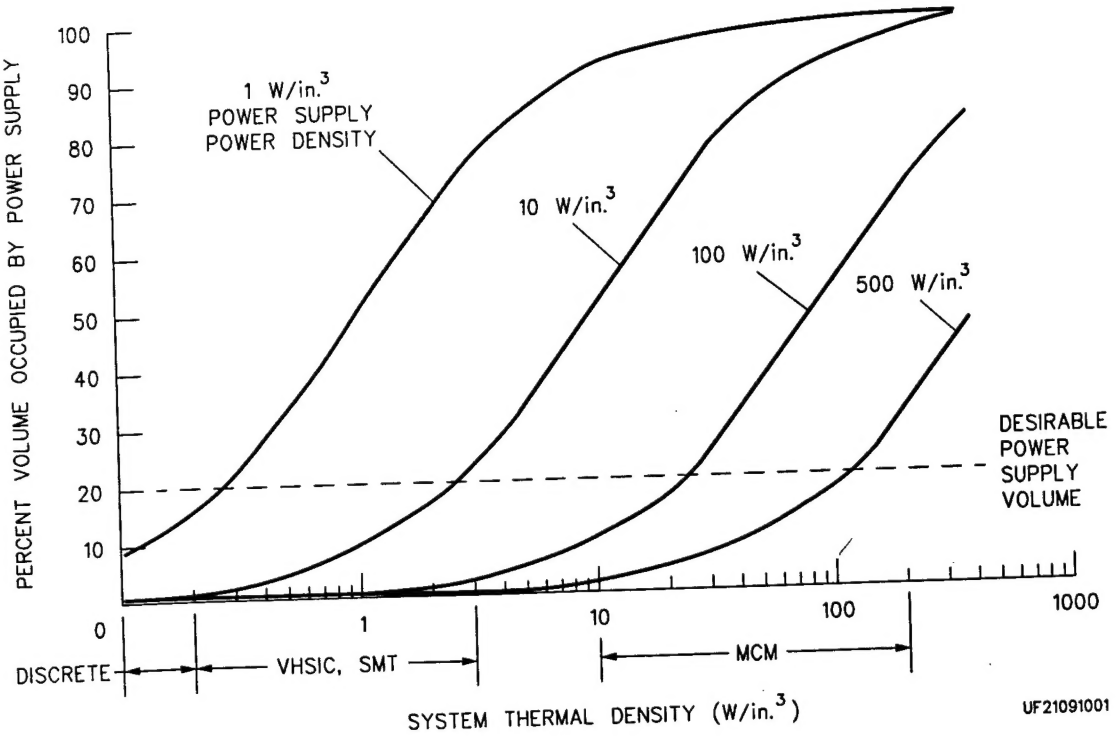

Figure 1. Power Supply Volume Versus System Thermal Density

rectification, using a silicon FET to eliminate this fixed drop, has dramatically improved rectification efficiency [1,2,3].

Figure 2 shows the implementation of a synchronous rectifier. Output diodes are replaced with switches and the switches are gated on and off as the diodes would normally conduct. The area of the switches is increased until either the cost of the synchronous rectifier becomes prohibitive, or the switching losses (ie.; gate drive, snubbing, cross conduction) equal the conduction losses. It has been shown when these two losses are equal, a minimum loss has been achieved [4]. Issues to be faced when considering synchronous rectification include:

- Snubbing of the Output Capacitance of the Device: In a conventional PWM circuit, the output capacitance of the synchronous rectifier will need to be snubbed the same as an ordinary diode giving rise to frequency related loss terms. In the circuit used for comparison in this paper, resonant operation was assumed where the synchronous rectifier output capacitance becomes part of the resonant circuit.

- Timing of the Gate Drive Signals: Improper timing of the synchronous rectifier can lead to overlapping conduction of the rectifiers. Cross conduction of the rectifiers may cause additional losses in the primary switch similar to reverse recovery losses due to output diodes. Cross conduction of the switches can also increase secondary currents, significantly increasing snubber requirements. In the topology considered, the transformer voltage changes slowly enough and the source impedance is high enough, there is not significant cross conduction losses.

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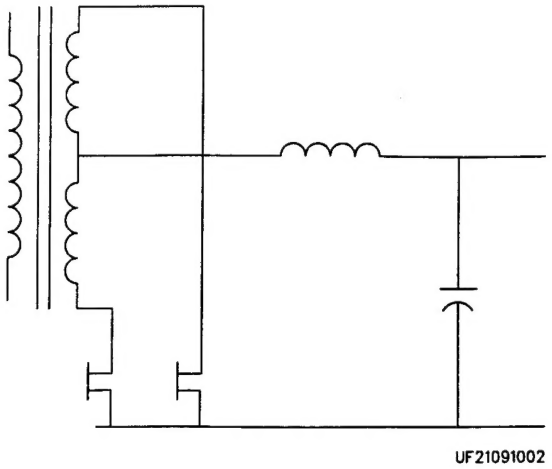

Figure 2. Output Rectification With Synchronous Rectifiers

- Connection of a Parallel Diode: If the gate drive does not provide continuous conduction of the output rectifiers, large voltage transients can be produced across the synchronous rectifiers. To control these transients, diodes are placed across the synchronous rectifiers. At high frequency, reverse recovery of these diodes becomes an issue and Schottky diodes are preferred. With UMOS or DMOS devices, the Schottky's need to be carefully selected so the MOSFET internal diode does not conduct. In the GaAs VFET structure, there is no parasitic diode and smaller (less capacitance) diodes can be used.

- Losses Due to Gate Resistance: Large gate resistance in the synchronous rectifier degrades efficiency in three ways. It limits how quickly the devices can be turned on and off, giving rise to gate drive timing uncertainty and the cross conduction problems described previously. If a resonant gate drive is used, the gate resistance degrades the circuit Q and losses. Finally, the drain voltage of the synchronous rectifier changes when it is not conducting, forcing current through the device's drain to gate capacitance. This current flows through the gate resistance producing additional loss. This puts a requirement of low gate resistance on the synchronous rectifier.

- Cost and Area of the Synchronous Rectifiers: Currently, synchronous rectifiers have found limited use due to the large silicon areas to achieve low drops. Typical HEXFET technology, with a 50-volt rating, produces about 2 m-ohm centimeter-squared specific resistance. To achieve a 0.20 volt drop at 50 amps requires 1.3 square centimeters of silicon or about six size 4 devices. DMOS technology promises to drop specific resistances to 0.5 m-ohm centimeter-squared. This paper reports even further reductions with silicon UMOS and GaAs VFET technology. Area requirements will drop significantly with these new technologies.

This paper reports rectifier development in support of a 100 watt per cubic inch, 95% efficient, 1.5 volt/67 amp power supply. To achieve the high power density requires moving the switching frequency into the 2 to 4 MHz range. A resonant topology is considered which allows

zero voltage turn on and turn off of the synchronous rectifier, minimizing snubbing requirements and easing the gate drive timing requirements. This paper presents the results of a trade study determining whether a synchronous rectifier based on silicon UMOSFETs or on GaAs VFETs would have a lower loss in a particular topology. An expression for minimum rectifier loss in this circuit is developed. A figure of merit is then defined which allows direct comparison of device dissipation. This figure of merit also allows the losses of a particular device to be minimized. Results of two dimensional modeling and device experiments for the two approaches support a comparison of the two technologies.

2.0 LOSS MECHANISMS AND MINIMIZATION

To properly compare the efficiency of the two rectifier technologies, the minimum loss of each approach needs to be calculated. This minimum is obtained by relating the loss mechanisms of the rectifiers to the die area. The minimum loss can be then be found by optimizing the die areas. A figure of merit can be developed by which different devices can be compared to find the one that results in minimum size for a given total power loss.

Synchronous rectifier loss fits into two categories, conduction loss and switching loss. In the case of synchronous rectifiers operated in a resonant circuit, driven by a center tapped transformer output, conduction loss (Pc) considered for a pair of rectifiers can be written;

$$Pc = Rsr\ I_0^2 \tag{1}$$

where Io = rms power supply output current
Rsr = Synchronous Rectifier Resistance

The rectifiers, when operated in a resonant circuit, will be switched with zero volts across them. Because the rectifiers switch with no voltage across them, the only switching loss that occurs is associated with the gate drive. Since a dissipative gate drive is being used, as much energy is lost in the drive circuit as is delivered to the gate. Assuming a low leakage gate capacitance, power dissipated as switching loss can be written;

$$Psw = f\ Ciss\ Vdr^2 \tag{2}$$

where Ciss = synchronous rectifier input capacitance
Vdr = peak gate drive voltage
f = supply operating frequency

For a pair of rectifiers, the gate switching loss is twice that shown above.

Other loss terms associated with switching loss and strongly influenced by the gate characteristics of the rectifier are: driver shoot-through loss, the loss caused by driving the driver input capacitance dissipatively, and the inefficiency of developing driver power. While these loss terms must be dealt with when attempting to minimize losses, this paper examines the simplified case where only the conduction loss (Pc) and gate switching loss (Psw) are included. This will

allow the derivation of a simple expression for the minimum loss. Total loss for a pair of rectifiers is in this case;

$$Pt = Pc + 2\ Psw \tag{3}$$

An expression can be developed to minimize the loss of a rectifier by relating resistance and input capacitance to area. This can be seen in Figure 3 which is a graph of the loss as a function of device input capacitance or more appropriately, die area. Resistance is inversely proportional to die area while input capacitance is directly proportionally. So the total resistance and capacitance can be written as a constant divided (or multiplied) by the area. This allows the expression of the total loss as a function of area. Substituting into equation (3), total loss is;

$$Pt = I_0^2\ Rsp/A + 2\ f\ Csp\ A\ Vdr^2 \tag{4}$$

where A = Die Area
Rsp = Specific Resistance
Csp = Specific Capacitance

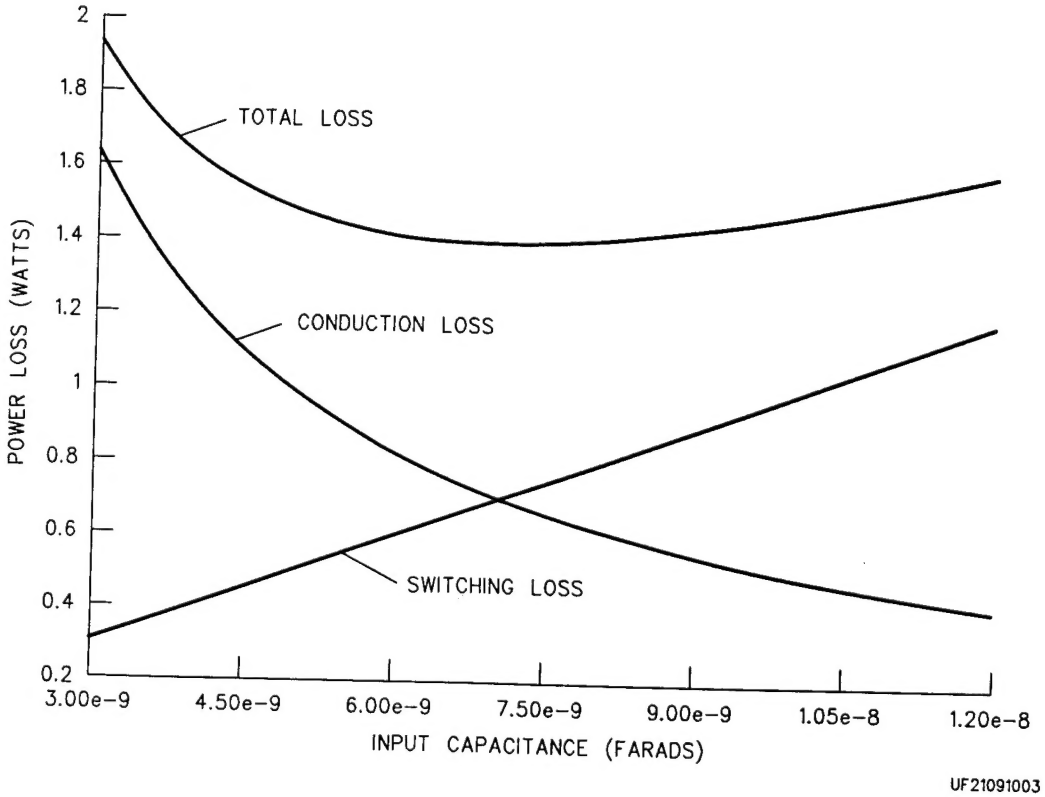

Figure 3. Rectifier Loss Versus Area

The loss equation can then be differentiated with respect to area and an optimum area can be found to be:

$$Aopt = Io\ (Rsp/2\ f\ Csp)^{1/2}/Vdr$$

The optimum loss can then be written as;

$$Pt\ \text{min.} = 2\ Io\ f^{1/2}\ (2\ Csp\ Rsp\ Vdr^2)^{1/2}$$

Previous work [3] defined a technology factor which was the product of device specific gate input-capacitance and specific on-resistance. This technology factor has been used as a figure of merit by which devices have been compared. This figure of merit, however, has the shortcoming that it is does not recognize specific resistance is a function of gate drive voltage or that switching losses can increase at higher drive levels. As the gate drive voltage increases, the on-resistance decreases. This allows a second level of optimization; there is a minimum loss where the product of the specific resistance, specific capacitance and gate drive voltage squared is minimum. This paper recommends a new figure of merit as;

$$Kcrq = Rsp\ Csp\ Vdr^2$$

which allows direct comparison of devices with varying gate drive requirements.

3.0 Silicon UMOSFET

Power MOSFETs with breakdown voltage in the 10-50 V range, operated as synchronous rectifiers, have been suggested to replace Schottky diodes in the output stage of power supplies for output voltages below 5 volts. These power MOSFETs must have the lowest possible specific on-resistance to minimize the conduction losses. It has already been theoretically and experimentally demonstrated that the UMOSFET structure is superior to the DMOSFET structure [5-9]. Most of the work has been devoted to devices that will support 50 volts with the lowest reported specific on-resistance of about 600 $\mu\Omega cm^2$ at a gate drive voltage of 20 volts. A power UMOSFET with a breakdown voltage of 30 volts has been also reported with a rather large specific on-resistance of 1370 $\mu\Omega cm^2$ for V_G = 10 V [5].

This section describes a new silicon power MOSFET structure, called modified mode field effect transistor (MODFET), having an ultralow on-resistance approaching 100 $\mu\Omega cm^2$ for a gate bias of 15 V and 200-450 $\mu\Omega cm^2$ for a gate bias of 5 V with a breakdown voltage of 25 V. This improved performance resulted from not only the inherent features of UMOSFET in eradicating the JFET pinching effect and increasing the cell packing density, but the unique feature of the MODFET where currents flow via an accumulation layer rather than spreading into the drift region.

The vertical cross sections of the proposed device (MODFET) and the conventional UMOSFET are shown in Figure 4. The principal difference is the presence of the extended gate which penetrates the n-drift region to the n+ substrate. The on-state current flows primarily along an accumulation layer formed on the trench sidewall. Unlike the conventional UMOSFET,

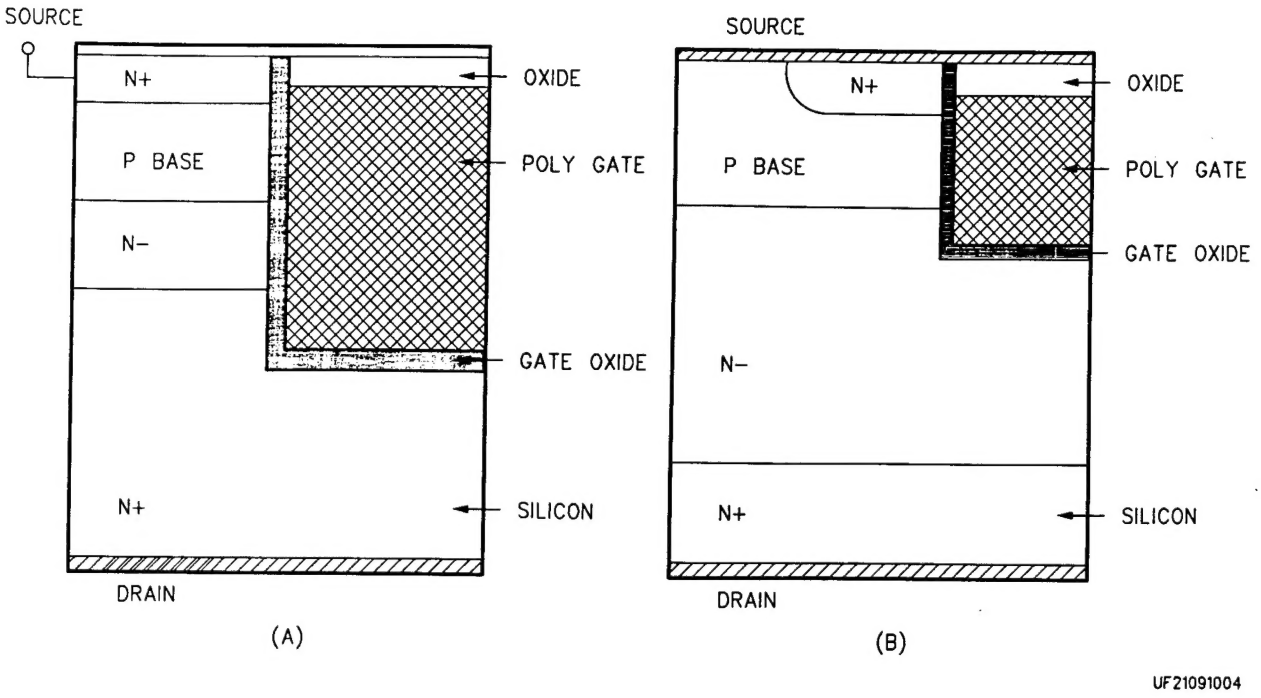

Figure 4. Cross Section Views of the New MODFET Structure (a) and the Conventional UMOSFET Structure (b)

the drift region resistance does not contribute to the on-resistance. As a result, the doping concentration can be as low as possible for the drift region. For this reason, the breakdown voltage of the MODFET device is determined by the punch through structure formed by the p-base/n-/n+ region as long as the oxide in the gate-drain overlapping region is sufficiently thick to support the voltage. For the conventional UMOSFET, however, an optimum doping concentration in the drift region must be used to achieve the desired breakdown voltage and reduce the on-resistance. With higher concentration, a deeper junction of the p-base region will be required to prevent reach-through breakdown due to the effect of concentration compensation. This is unlikely in the MODFET devices because of the difference in doping concentration between the p-base and n-drift regions. The measured electrical properties of fabricated devices for two cases (MODFET A and B) are presented in Table 1. The typical output I-V characteristics for one of the devices is shown in Figure 5. About 21-24 V drain to source breakdown voltages (BV) were observed in the off state and the measured threshold voltages (V_T) were in the 1 V range. The specific on-resistances were measured at a pulsed gate bias of 5 volts. Although lower on-resistance can be obtained using higher gate biases, a 5 V gate bias was chosen to reduce gate drive losses for the synchronous rectifier application. Since a planarization technique for polysilicon was not available, a remote region having a shortened n+/p-base structure was employed with the source contact located outside the trench regions as indicated by the side contact in Figure 4a. To account for the additional resistances caused by the lateral current flow in the n+ region, two dimensional numerical simulations were carefully performed using parameters measured from the fabricated test elements. These results were in excellent agreement with each other and, hence, adopted to determine the specific on resistance.

TABLE 1. COMPARISON OF THEORETICAL AND EXPERIMENTAL RESULTS FOR THE FABRICATED DEVICE AT A GATE BIAS OF 5 VOLTS

Device	Specific On Resistance, $R_{on,sp}$		
	Numerical	Analytical	Experimental
MODFET A t_{ox} = 720 Å	291 BV = 25 V V_T = 1.5 V	297 BV = 21 V V_T = 1.3 V	430 BV = 21 V V_T = 1.3 V
MODFET B t_{ox} = 370 Å	159 BV = 25 V V_T = 1.5 V	164 BV = 22 V V_T = 1.2 V	230 BV = 22 V V_T = 1.2 V
UMOSFET C t_{ox} = 500 Å (V_G = 10 V)	—	—	1370 BV = 30 V
UMOSFET D t_{ox} = 700 Å (V_G = 20 V)	—	—	580 BV = 50 V

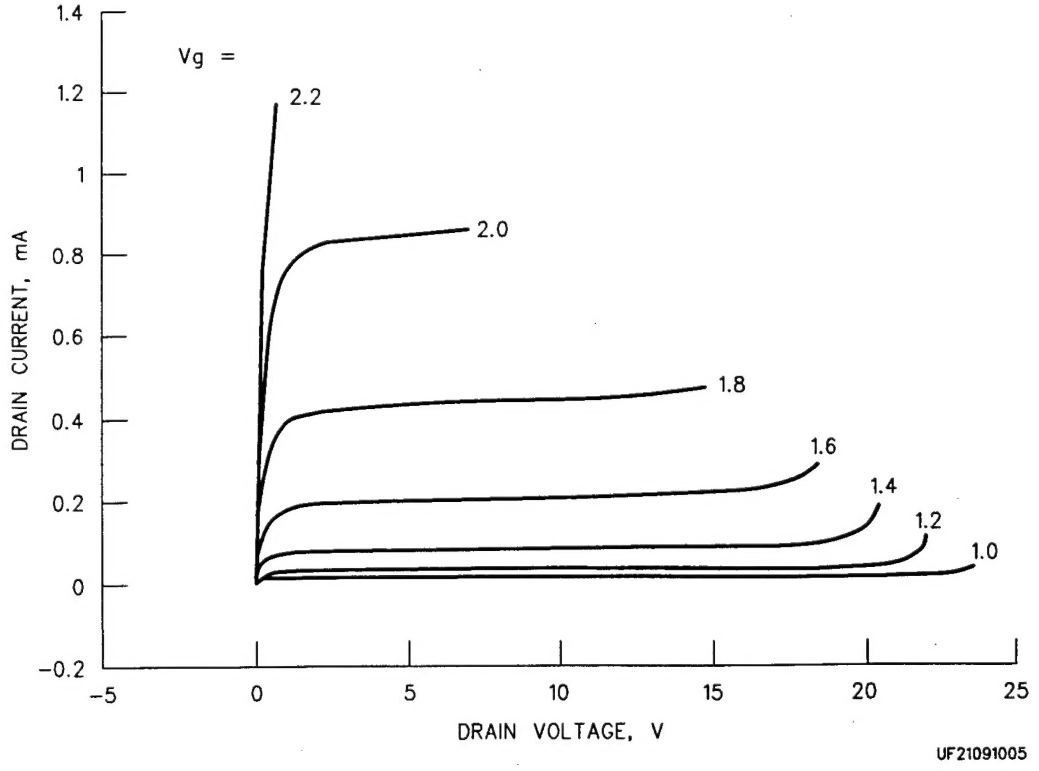

Figure 5. The Typical Output I-V Characteristics for the Fabricated Device Capable of Supporting 24 Volts Drain Voltage

From the experimental results, the $R_{on,sp}$ increases as the gate oxide thickness (t_{ox}) increases (see Table I), and decreases with the reduced p-base junction depth (shorter inversion channel) due to the lower electron mobility in the inversion region as compared with the accumulation region. This trend is also seen in the simulations and analytical calculations. The present data show that the experimental $R_{on,sp}$ is about 1.4 times higher than the simulated one. Using a thinner gate oxide and better control of RIE-induced damage by process refinement could improve the channel mobility and thus reduce the specific on-resistance even further.

Data on two previously reported devices (UMOSFET C [5] and D [9]) are also compared in Table 1. The gate drive voltage for these devices is much higher than that used to obtain the data for the MODFET devices. When this factor is taken into account, it can be concluded that the MODFET structure is superior to the conventional UMOSFET structure by a factor of 2 to 4 times.

4.0 GaAs Device

For high frequency and high current switching vertical channel FETs, or VFETs, are another choice. The basic VFET structure, also called static induction transistor(SIT) [10],[11], is shown in Figure 6. Due to its multichannel conduction, the VFET generally has higher current handling capability per unit area than DMOS and UMOS under the same breakdown voltage requirement. High power 1-GHz operation was demonstrated [12] in silicon VFET technology using a diffused surface gate design. Theoretically, VFETs fabricated from GaAs should have another factor 4 to 8 higher current switching capability than silicon VFETs [13]. However, neither GaAs VFETs using a buried gate [14] nor a Schottky gate structure [15] could realize the performance predicted by theoretical calculation. This was caused by the process difficulty of fabricating GaAs VFETs with both low gate and low source resistance. This difficulty was overcome recently at Texas Instruments. Using a buried gate structure, with 1 amp GaAs VFETs were designed and fabricated resulting with the following performance.

Voltage Gain:	> 4
On-resistance:	< 68 mohms at Vg = 0 volts
Gate capacitance:	< 336 pF at Vg = 0 volts
Gate resistance:	< 3 ohms
Switching time:	< 2 nS at Id = 1 ampere

5.0 Conclusions

Table 2 presents a comparison of the theoretical and measured silicon and GaAs output rectifier performance. When used as an output rectifier in a resonant power supply operating at 2.5 MHz and with a dissipative drive, it is predicted that a GaAs VFET will have 1.4 watts of loss compared to over 5 watts for the silicon device. Measured performance has not quite reached the theoretical predictions. As expected, the more mature silicon experimental device is closer to its theoretical limits than the GaAs device. Both experimental results indicate that there is good correlation with prediction, and that high efficiency rectification is achievable. Table 2 also shows device switching times of the GaAs have been demonstrated to be better than 2 nanoseconds. Our construction techniques limited the silicon device switching speeds so we were not able to do a comparison.

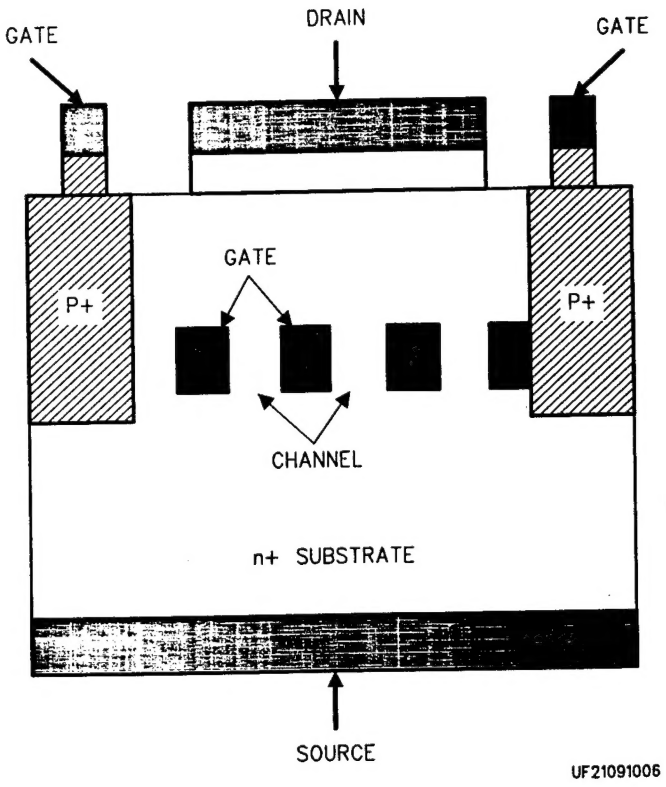

Figure 6. Cross Section of GaAs Device

TABLE 2. COMPARISON OF SYNCHRONOUS RECTIFIER TECHNOLOGIES

	Silicon		GaAs	
	Theory	**Actual**	**Theory**	**Actual**
Blocking Voltage (V)	30	20-25	20	12
Specific Resistance (μ-ohm-cm^2)	352	453	43	96
Specific Capacitance (nF/cm^2)	50	--	52	80
Drive Voltage (V)	5	5	3	3
Switching Time (nS)	--	--	<2	<2
$R_{sp} * C_{sp} * V_{drive}^2$ (E-12)	440	563	20	69
Loss with Dissipative Drive (W)	6.6	7.5	1.4	2.6

This paper presented a theoretical and experimental comparison of silicon and GaAs synchronous rectifiers. Optimum silicon UMOSFET and GaAs VFET structures were described. Predicted performance based on two dimensional simulations and analytical models were presented. GaAs was found to have a predicted figure of merit ten times better than silicon leading to one third the losses in the GaAs parts. Experimental devices were constructed to verify the analysis and test results from these devices is presented. Good correlation was achieved between the calculations and measurements. Based on these calculations and experiments, GaAs will play a key role in maximizing the efficiencies of low voltage power supplies.

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